In the Claims

This claim set replaces all previous versions of the claims:

1. (Currently Amended) An integrated circuit switch comprising:

at least two signal ports coupled by a signal path, the signal path including a channel of at least one series FET;

a shunt path coupled to ground and including a channel of a shunt FET;

a first control signal applied to the signal path; and,

a second control signal applied directly to both a gate terminal of the series FET and to a drain terminal of the shunt FET[[,]] to control the on/off states of the shunt and series FETs,

wherein the second control ~~voltage~~ signal, the drain terminal of the shunt FET, and the gate terminal of the series FET are directly and continuously coupled to each other.

2. (Previously Presented) A method for switching a signal so as to selectively connect a first port in an integrated circuit to a second port in the integrated circuit, comprising:

providing a series switch in a signal path between the first port and the second port;

providing a shunt switch in a shunt path coupled to ground;

directly and continuously coupling the drain terminal of the shunt switch to the gate terminal of the series switch and to a common logic signal source;

providing a first control voltage applied to the signal path; and,

using a common logic signal provided by the common logic signal source to control both the series switch and the shunt switch.

Claims 3 – 5. (Canceled)

6. (Previously Presented) A switch for coupling a first port to a second port, comprising:

a first control signal input;

a second control signal input coupled between the first port and the second port;

a FET connected in series between the first port and the second port, said series FET having a gate terminal coupled to the first control signal input; and

means for enhancing the isolation between the first and second ports, and for improving the harmonic noise rejection of the switch, the isolation and harmonic rejection means having an input coupled to the first control signal input and to the gate of the series FET, whereby a single control signal is applied to both the series FET and the isolation and harmonic rejection means, via the first control signal input, in order to turn the series FET on and simultaneously turn the isolation means off and, conversely, in order to turn the series FET off and simultaneously turn the isolation means on, said means for enhancing isolation and improving harmonic noise rejection including a shunt FET with a drain terminal directly and continuously coupled to the gate terminal of the series FET and to the first control signal input.

7. (Original) The switch of Claim 6, wherein the isolation and harmonic rejection means includes a

shunt path including a shunt FET, the shunt FET having a drain coupled to the control signal input and to the gate of the series FET, whereby the single control signal is applied to both the series FET and the shunt FET, via the control signal input, in order to turn the series FET on and simultaneously turn the shunt FET off and, conversely, in order to turn the series FET off and simultaneously turn the shunt FET on, the harmonic rejection is provided without the need of a separate feedforward capacitor.

8. (Previously Presented) A method of controlling the coupling of a first port to a second port via a series/shunt FET switch, comprising the steps of:

providing a first control voltage between the first port and the second port;

directly and continuously coupling a drain terminal of a shunt FET to a gate terminal of a series FET and to a control signal source;

isolating the first port from the second port, using a single control signal provided by the control signal source, by turning off the series FET by biasing the gate-source voltage of the series FET below the pinchoff voltage, and by turning the shunt FET on by biasing the gate-source voltage above the pinchoff voltage; and

coupling the first port to the second port, using a single control signal provided by the control signal source, by turning on the series FET by biasing the gate-source voltage above the pinchoff voltage, and turning the shunt FET off by biasing the gate-source voltage below the pinchoff voltage.

9. (Previously Presented) An integrated circuit for selectively connecting and disconnecting a first

RF port to or from a second RF port, comprising:

a signal path connecting the first RF port and the second RF port;

a first control electrode coupled to the signal path;

at least one series switching transistor having a signal path and a second control electrode, a first control voltage applied to the second control electrode permitting a signal to pass, a second control voltage applied to the second control electrode rendering the current path to be of high impedance; and

a shunt transistor having a diverging signal path, one end of the signal path of the shunt transistor coupled to the second control electrode of said at least one series switching transistor, a second end of the signal path of the shunt transistor coupled through a low signal impedance to the signal ground reference; additionally allowing for control of the shunt transistor signal path impedance by application of the first control voltage to both the second control electrode of the series switching transistor and simultaneously to the drain and/or source of the shunt transistor rendering the signal path of the shunt transistor substantially nonconductive while the series switching transistor signal path is conductive, and wherein application of the second control voltage to the shunt transistor renders the signal path of the shunt transistor conductive while the series switching transistor path is simultaneously nonconductive with the same second control voltage simultaneously applied to its second control electrode to thereby increase the isolation between the first and second RF ports,

wherein a drain of said shunt transistor is directly and continuously coupled to a gate terminal of said series transistor and to a source of the first and second control voltages.

10. (Previously Presented) The integrated circuit of Claim 9, wherein said at least one switching transistor is a field effect transistor.

11. (Original) The integrated circuit of Claim 9, wherein said at least one switching transistor is an insulated gate field effect transistor.

12. (Canceled)

13. (Original) The integrated circuit of Claim 9, wherein the shunt transistor is a field effect transistor.

14. (Original) The integrated circuit of Claim 13, wherein the shunt transistor is an insulated gate field effect transistor.

15. (Previously Presented) The integrated circuit of Claim 14, wherein a drain of the shunt transistor is coupled to the second control electrode of said at least one switching transistor, the first and second control voltages being applied to the drain.

Claims 16 – 17. (Canceled)

18. (Original) The integrated circuit of Claim 9, wherein the signal path of the shunt transistor is coupled to the signal ground reference through a shunt capacitor.

19. (Previously Presented) The integrated circuit of Claim 9, wherein the first control voltage provides a voltage differential across the series switching transistor.

Claims 20 – 23. (Canceled)